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09/606,200	06/29/2000	Govind Malalur	P108339-09064	8167

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EXAMINER	
LEE, TIMOTHY L	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 10/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,200	MALALUR, GOVIND	
	Examiner	Art Unit	
	Timothy Lee	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,33-35,37,38,40-43,46,49,50 and 53-58* is/are rejected.

7)☒ Claim(s) *24-32,36,39,44,45,47,48,51 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities: The status of the application 09/343,409 cited on page one of the specification must be updated.

Appropriate correction is required.

3. The abstract of the disclosure is objected to because "be snooping," in lines 2-3, should be corrected to "by snooping." Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 4,424,565) in view of Warner et al. (US 6,289,015).

6. Regarding claims 1 and 53, Larson discloses a channel interface circuit in a multiprocessor environment to provide a high speed interface between a processor and the communication channel which interconnects all the processors. Fig. 7 illustrates some typical table loading contents of DMA control table 107, which circuit functions as a hardware address

generator. State controller 104 activates lead ENABLE either upon receipt of a match signal or upon the completion of the data message and the receipt of an appropriate signal from error checker 103 on lead STATE, indicating the receipt of an error free message (DMA descriptor including a reload field). See col. 9, lines 53-63. An update method is to have DMA transfer unit 108 update the data in DMA control table 107 to reflect the new starting address for data stored based on the data message just stored in processor memory 201 (identifying a location of a next DMA descriptor based upon the condition of the reload field). See col. 10, lines 6-23. In loading the table, the processor 200, by applying appropriate signals on the processor control and address buses, enables memory device 111 to receive and store data from the processor data bus. See col. 5, lines 64-67. Based on this, the processor does not have to use the communications channel 101 to communicate with the table (CPU access to the lookup table without requiring communication on the communication channel). See also the connection diagram on Figs. 1 and 2. Larson does not expressly disclose snooping the communication channel for lookup table information.

7. Warner et al. discloses a process of constructing a lookup table, called the "learning" of addresses by the switch 60. The address lookup device snoops the bus for the purpose of learning both the source and the destination addresses of the received packet (constructing a table by snooping a communication channel in a network switch for lookup table information). See col. 6, lines 32-35. Once an address/port record has been created in the address-lookup table 100, the switch 60 is able to make a determination as to which port a packet having a "learned" destination address should be routed. The address-lookup device is also shown to be coupled to

an EEPROM 104 (transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory). See col. 4, line 47-col. 5, line 18.

8. It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the "learning" ability found in Warner et al. into the DMA storage system of Larson. One would have been motivated to do this because the table needs to be updated periodically to reflect changes in network configuration that can occur when nodes are added or deleted from the system. Sending a packet to a destination that no longer exists is a waste of resources.

9. Regarding claim 2, it is inherent in the purpose of snooping disclosed by Warner et al. that the lookup information will include insert messages for newly found addresses and delete messages for addresses that are found to be no longer active.

10. Regarding claim 3, as mentioned previously, Larson discloses that if the ENABLE signal is set to a certain way, the DMA will continue loading information into certain addresses of the table.

11. Regarding claim 4, as mentioned previously, Larson discloses that the table is connected to a processor.

12. Regarding claim 5, if the ENABLE is not set in Larson, then it is possible that DMA operations will occur starting at another location. It depends on the type of class and the type of the message. See col. 10, lines 2-15 and col. 10, lines 44-50.

13. Regarding claim 6, as shown in Fig. 2 of Larson, the processor interacts with various memories, including the processor memory (system memory is dedicated for CPU operation).

14. Regarding claim 7, neither Larson nor Warner et al. discloses synchronizing multiple lookup tables, but it would have been obvious to do so in the combined system of Larson and Warner et al.. One would have been motivated to do this because it would be very inefficient to have multiple tables each have different information contained in them and have to figure out which table has the most up-to-date information.

15. Claims 8-16 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warner et al. (US 6,289,015) in view of O'Donnell et al. (US 6,381,642).

16. Regarding claims 8 and 54, Warner et al. discloses a process of constructing a lookup table, called the "learning" of addresses by the switch 60. The address lookup device snoops the bus for the purpose of learning both the source and the destination addresses of the received packet (constructing a table by snooping a communication channel in a network switch for lookup table information). See col. 6, lines 32-35. Once an address/port record has been created in the address-lookup table 100, the switch 60 is able to make a determination as to which port a packet having a "learned" destination address should be routed. The address-lookup device is also shown to be coupled to an EEPROM 104 (transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory). See col. 4, line 47-col. 5, line 18. Warner et al. does not expressly disclose monitoring port activity in the network switch.

17. O'Donnell et al. discloses an in-band method for reporting operational statistics relative to the ports of a switch. The F_ports of a FC switch have a number of statistical counters or port counters associated therewith. These port counters are used to monitor operational parameters, such as bandwidth, error statistics, and various operational characteristics of the associated

F_port (monitoring port activity by storing port activating in a statistics register, reading the port activity data with a statistics gathering unit). See col. 2, lines 47-52. The management director 24 of Fig. 1 generates statistical information concerning the performance of links 17 that connect internal port 16 to the various F_ports. This statistical information is presented to host client 13 in the format of a Monitor information record 45. Management-director 24 maintains a plurality of sets of statistical counters, each set of which corresponds to one of a like plurality of F_ports. In addition, management director may maintain a set of statistical counters for internal port 16.

18. It would have been obvious to combine the port monitoring functions of O'Donnell et al. with the system of Warner et al. In this combined system, the monitoring data could be stored in the RAM of Warner et al. (transmitting the port activity data directly to a remote system memory...reconstructing the statistics register in the remote system memory and then accessing the remote system memory with a remote CPU to read the reconstructed statistics register). One would have been motivated to do this because it is important to keep track of how each port is performing so that if a failure occurs, the switch doesn't continue to try to send data over the broken link, which would lead to inefficiency in the system.

19. Regarding claim 9, it is inherent in the purpose of snooping disclosed by Warner et al. that the lookup information will include insert messages for newly found addresses and delete messages for addresses that are found to be no longer active.

20. Regarding claim 10, neither Warner et al. nor O'Donnell et al. discloses using DMA in transferring the port activity data, but it would have been obvious to use DMA to do. One would have been motivated to do this because DMA operations would simplify the process of transferring information.

21. Regarding claim 11, in Warner et al., a special address-lookup device looks up information in the address table, and inherently, this device is a type of CPU. See col. 4, lines 54-65.

22. Regarding claims 12 and 14, concerning port monitoring, O'Donnell et al. discloses that it can be done at predetermined intervals. It is inherent that the time intervals would be counted in terms of clock cycles. See claim 3.

23. Regarding claim 13, in Warner et al., the DRAM exists to store the table and for running the processor.

24. Regarding claim 15, neither O'Donnell et al. nor Warner et al. discloses synchronizing multiple lookup tables, but it would have been obvious to do so in the combined system of O'Donnell et al. and Warner et al.. One would have been motivated to do this because it would be very inefficient to have multiple tables each have different information contained in them and have to figure out which table has the most up-to-date information.

25. Regarding claim 16, neither O'Donnell et al. nor Warner et al. discloses picking one of the plurality of statistics registers to use, but it would have been obvious to do so in the combined system of O'Donnell et al. and Warner et al.. One would have been motivated to do this because allowing the system to pick any of the statistics registers makes for better efficiency.

26. Claims 17-22 and 55are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 4,424,565) in view of O'Donnell et al.

27. Regarding claims 17 and 55, Larson discloses a channel interface circuit in a multiprocessor environment to provide a high speed interface between a processor and the communication channel which interconnects all the processors. Fig. 7 illustrates some typical

table loading contents of DMA control table 107, which circuit functions as a hardware address generator. State controller 104 activates lead ENABLE either upon receipt of a match signal or upon the completion of the data message and the receipt of an appropriate signal from error checker 103 on lead STATE, indicating the receipt of an error free message (DMA descriptor including a reload field). See col. 9, lines 53-63. An update method is to have DMA transfer unit 108 update the data in DMA control table 107 to reflect the new starting address for data stored based on the data message just stored in processor memory 201 (identifying a location of a next DMA descriptor based upon the condition of the reload field). See col. 10, lines 6-23. In loading the table, the processor 200, by applying appropriate signals on the processor control and address buses, enables memory device 111 to receive and store data from the processor data bus. See col. 5, lines 64-67. Based on this, the processor does not have to use the communications channel 101 to communicate with the table (CPU access to the lookup table without requiring communication on the communication channel). See also the connection diagram on Figs. 1 and 2. Larson does not expressly disclose port monitoring.

28. O'Donnell et al. discloses an in-band method for reporting operational statistics relative to the ports of a switch. The F_ports of a FC switch have a number of statistical counters or port counters associated therewith. These port counters are used to monitor operational parameters, such as bandwidth, error statistics, and various operational characteristics of the associated F_port (monitoring port activity by storing port activating in a statistics register, reading the port activity data with a statistics gathering unit). See col. 2, lines 47-52. The management director 24 of Fig. 1 generates statistical information concerning the performance of links 17 that connect internal port 16 to the various F_ports. This statistical information is presented to host client 13

in the format of a Monitor information record 45. Management-director 24 maintains a plurality of sets of statistical counters, each set of which corresponds to one of a like plurality of F_ports. In addition, management director may maintain a set of statistical counters for internal port 16.

29. It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the port monitoring features of O'Donnell et al. into the system of Larson. One would have been motivated to do this because it is important to keep track of how each port is performing so that if a failure occurs, the switch doesn't continue to try to send data over the broken link, which would lead to inefficiency in the system.

30. Regarding claim 18, as mentioned in Larson, the processes involving storage of information are controlled through DMA.

31. Regarding claim 19, as mentioned previously, Larson discloses that if the ENABLE signal is set to a certain way, the DMA will continue loading information into certain addresses of the table.

32. Regarding claims 20 and 21, concerning port monitoring, O'Donnell et al. discloses that it can be done at predetermined intervals. It is inherent that the time intervals would be counted in terms of clock cycles. See claim 3.

33. Regarding claim 22, neither O'Donnell et al. nor Larson discloses picking one of the plurality of statistics registers to use, but it would have been obvious to do so in the combined system of O'Donnell et al. and Larson. One would have been motivated to do this because allowing the system to pick any of the statistics registers makes for better efficiency.

34. Claims 46, 49, 50, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 4,424,565) in view of O'Donnell et al, further in view of Bellanger (US 6,256,306)

and in light of the rejection to claim 17. Neither Larson nor O'Donnell expressly discloses using tags for processing the packet.

35. Regarding claims 46 and 58, Bellenger discloses a network switch that involves tagging. Flow detect logic is coupled with the set of ports on the switch node, which monitors frames received by the set of ports and generates an identifying tag for use in accessing the route table memory. The tags act as flow signatures to associate a frame with a sequences of frames traversing the switch (inserting a stack specific tag into a packet). The identifying tag is used to access the route table memory (processing the packet in a stack of switches in accordance with the tag information). Switch route data is retrieved from the route table memory. This data is used to generate a switch route field fro the frame. See col. 3, lines 10-60. Bellinger does not expressly disclose removing the tag, but it would have been obvious to remove the tag after the proper information had been retrieved using the tag. One would have been motivated to do this because the tag would have served its purpose after the retrieval of information, and it would be more efficient to send a streamlined packet along the data routes. It would have been obvious to combine the tag processing of Bellanger into the combined system of Larson and O'Donnell et al.. One would have been motivated to do this because using the tags can be more efficient in processing the packets than just by processing information found in the headers. The tags are smaller are more easily detected and processed.

36. Regarding claims 49 and 50, concerning port monitoring, O'Donnell et al. discloses that it can be done at predetermined intervals. It is inherent that the time intervals would be counted in terms of clock cycles. See claim 3.

37. Claims 23, 33, 34, 35, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 4,424,565) in view of Warner et al., further in view of Bellanger (US 6,256,306) and in light of the rejection to claim 1.

38. Regarding claims 23 and 56, Neither Larson nor Warner et al. expressly discloses using tags for processing the packet. Bellenger discloses a network switch that involves tagging. Flow detect logic is coupled with the set of ports on the switch node, which monitors frames received by the set of ports and generates an identifying tag for use in accessing the route table memory. The tags act as flow signatures to associate a frame with a sequences of frames traversing the switch (inserting a stack specific tag into a packet). The identifying tag is used to access the route table memory (processing the packet in a stack of switches in accordance with the tag information). Switch route data is retrieved from the route table memory. This data is used to generate a switch route field fro the frame. See col. 3, lines 10-60. Bellinger does not expressly disclose removing the tag, but it would have been obvious to remove the tag after the proper information had been retrieved using the tag. One would have been motivated to do this because the tag would have served its purpose after the retrieval of information, and it would be more efficient to send a streamlined packet along the data routes. It would have been obvious to combine the tag processing of Bellanger into the combined system of Larson and Warner et al.. One would have been motivated to do this because using the tags can be more efficient in processing the packets than just by processing information found in the headers. The tags are smaller are more easily detected and processed.

39. Regarding claim 33, it is inherent in the purpose of snooping disclosed by Warner et al. that the lookup information will include insert messages for newly found addresses and delete messages for addresses that are found to be no longer active.

40. Regarding claims 34 and 35, it is inherent that a central processor is used in searching for the address locations. Also, as mentioned previously, multiple memories exist, so one could be used for the processor.

41. Claims 37, 38, 40-43, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warner et al. in view of O'Donnell et al., further in view of Bellanger (US 6,256,306) and in light of the rejection to claim 8.

42. Regarding claims 37 and 57, neither O'Donnell et al. nor Warner et al. expressly discloses using tags for processing the packet. Bellenger discloses a network switch that involves tagging. Flow detect logic is coupled with the set of ports on the switch node, which monitors frames received by the set of ports and generates an identifying tag for use in accessing the route table memory. The tags act as flow signatures to associate a frame with a sequences of frames traversing the switch (inserting a stack specific tag into a packet). The identifying tag is used to access the route table memory (processing the packet in a stack of switches in accordance with the tag information). Switch route data is retrieved from the route table memory. This data is used to generate a switch route field fro the frame. See col. 3, lines 10-60. Bellinger does not expressly disclose removing the tag, but it would have been obvious to remove the tag after the proper information had been retrieved using the tag. One would have been motivated to do this because the tag would have served its purpose after the retrieval of information, and it would be more efficient to send a streamlined packet along the data routes. It would have been obvious to

combine the tag processing of Bellanger into the combined system of Warner et al. and O'Donnell et al.. One would have been motivated to do this because using the tags can be more efficient in processing the packets than just by processing information found in the headers. The tags are smaller are more easily detected and processed.

43. Regarding claim 38, it is inherent in the purpose of snooping disclosed by Warner et al. that the lookup information will include insert messages for newly found addresses and delete messages for addresses that are found to be no longer active.

44. Regarding claims 40 and 42, it is inherent that a central processor is used in searching for the address locations. Also, as mentioned previously, multiple memories exist, so one could be used for the processor.

45. Regarding claims 41 and 43, concerning port monitoring, O'Donnell et al. discloses that it can be done at predetermined intervals. It is inherent that the time intervals would be counted in terms of clock cycles. See claim 3.

Allowable Subject Matter

46. Claims 24-32, 36, 39, 44, 45, 47-48, and 51-52 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Marthy et al. (US 5,610,905) and Earnest et al. (US 6,092,116) discloses systems that either deal with DMA or port monitoring.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy Lee whose telephone number is (703)305-7349. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703)305-4744. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

TLL

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